Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1.   (Currently Amended) A method of matching impedances across ~~reducing impedance variations in~~ an electrical circuit configured for placement on an integrated circuit (IC) ~~including substrate~~, the electrical circuit including an electrical component having (i) input and output ports and (ii) a plurality of interconnected cascaded impedance devices configured for connection along a feedback path formed between the input and output ports, each impedance device having a predetermined ~~an~~ impedance value, the method comprising:

forming groups of resistors, each group (i) corresponding to one of the impedance devices, (ii) including two or more resistor paths, and (iii) having a combined impedance value substantially equal to the impedance value of its corresponding device; and

configuring the groups of resistor paths to form an interdigital structure across a substrate when the IC is placed thereon, the interdigital structure being formed when the resistor paths split at one point on the substrate and recombine at another point.

2. (Previously Presented) An apparatus for matching impedances across an integrated circuit (IC) including a plurality of interconnected impedance devices, each device having an impedance value, the apparatus comprising:

means for forming groups of resistors, each group (i) corresponding to one of the impedance devices, (ii) including two or more parallel resistor paths, and (iii) having a

combined impedance value substantially equal to the impedance value of its corresponding device; and

means for configuring the groups of parallel resistor paths to form an interdigital structure across a substrate when the IC is placed thereon, the interdigital structure being formed when the parallel resistor paths split at one point on the substrate and recombine at another point.

3. (Previously Presented) The apparatus of claim 2, wherein the IC comprises a programmable gain amplifier (PGA).

4. (Original) The apparatus of claim 3, wherein the PGA is a differential amplifier.

5. (Previously Presented) The apparatus of claim 4, wherein the impedance values of all of the impedance devices are substantially equal.

6. (Original) The apparatus of claim 5, wherein the IC is formed in CMOS.